High Resolution Inner Vertex Detector

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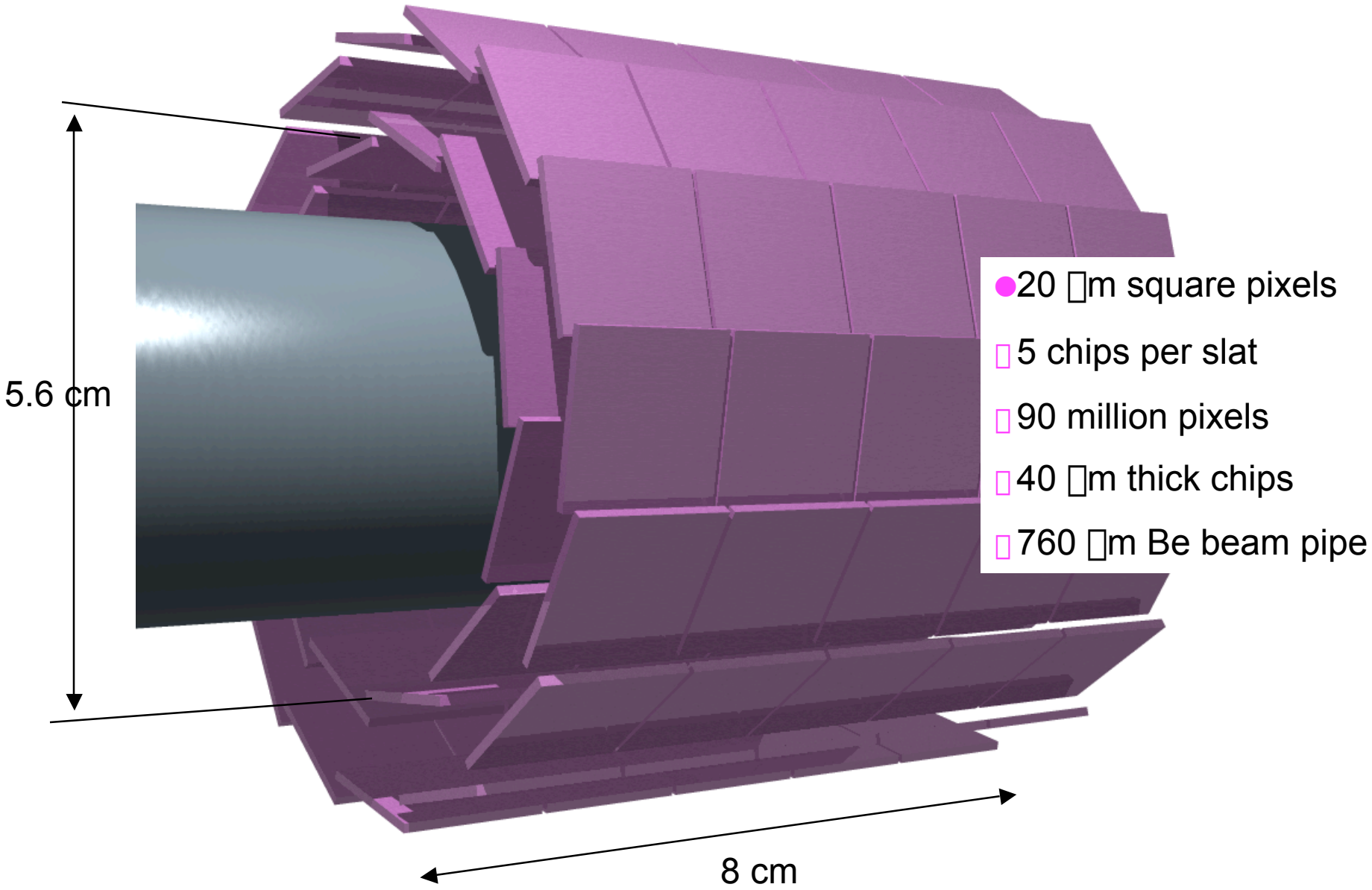
Motivation for an inner tracker

- Measure D mesons, charm quark production
- Emphasized in the long range plan for STAR
  - » Window to early hot parton phase
    - – Large mass, c quarks less less likely from later mixed phase and hadron phase
    - – More restrictive than measure of strange quark production
    - – Augments measurements of multi-strange particles, Ω^-
    - – Calibration of J/ψ suppression

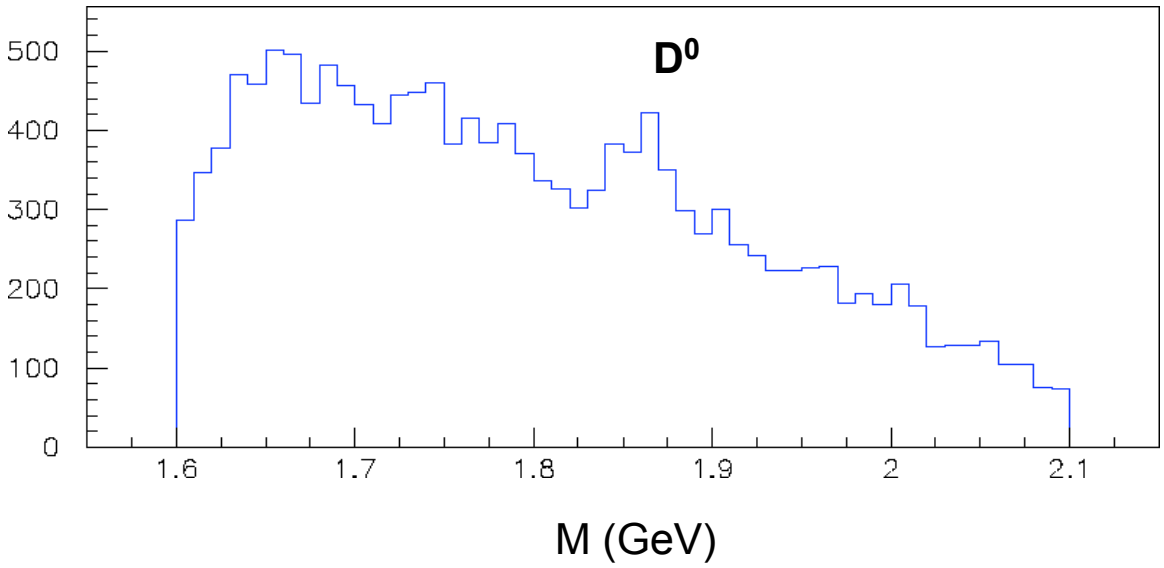
Technical Challenge of D mesons

- Topological separation of D vertex from primary vertex with thousands of tracks
  - » $D^+ \to K^- \pi^+ \pi^+$ 8% $c\tau = 320\ \mu m$
  - » $D^0 \to K^- \pi^+$ 3.65% $c\tau = 125.9\ \mu m$
- Require microscopic vertex resolution
  - » minimum coulomb scattering
  - » Minimum distance to interaction to improve pointing resolution
    - – Therefore need excellent two track resolution
  - » excellent position resolution

Active Pixel Sensor (APS)



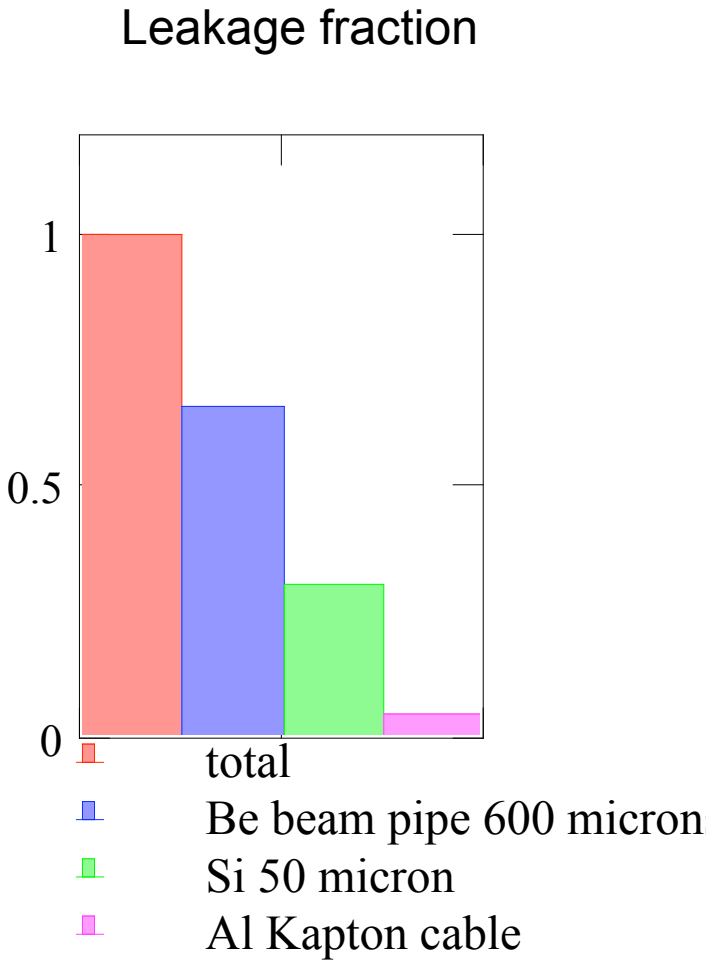
Invariant mass reconstruction of D^0s □ k □ (preliminary simulation)



- 250,000 events
- 5 D^0s in –1<□<+1
- Would need 6X10^6 if 1 D^0
  - » This is 2 weeks running

$$N = \frac{B}{s^2}$$

Rejection of primary tracks



- For large rejection ratios must set cut at several times multiple scattering angle
- At these large angles single coulomb scattering dominates and materials contribute linearly

Beam pipe x/X0 = .17 %
Si x/X0 = .05 %

Operating in the RHIC environment

- Very central collision dN/dη = 700
- Resulting hit density on inner vertex: 14 hits/cm^2
- Fraction of pixels filled in a single central event at the inner radius = 0.05%

R&D effort focusing on APS in CMOS

- Can be thinned like CCDs
- Better radiation hardness
- Potentially fast readout and lower power since zero suppression can be done on the detector chip
- Design freedom with standard industry process
- LEPSI demonstrated technology with minimum ionizing particles
- No CMOS APS detectors operating in an experiment
- MIP detection depends on a feature of the CMOS process that could disappear, although latest word from LEPSI is that epi layer is not necessary

LBNL R&D so far

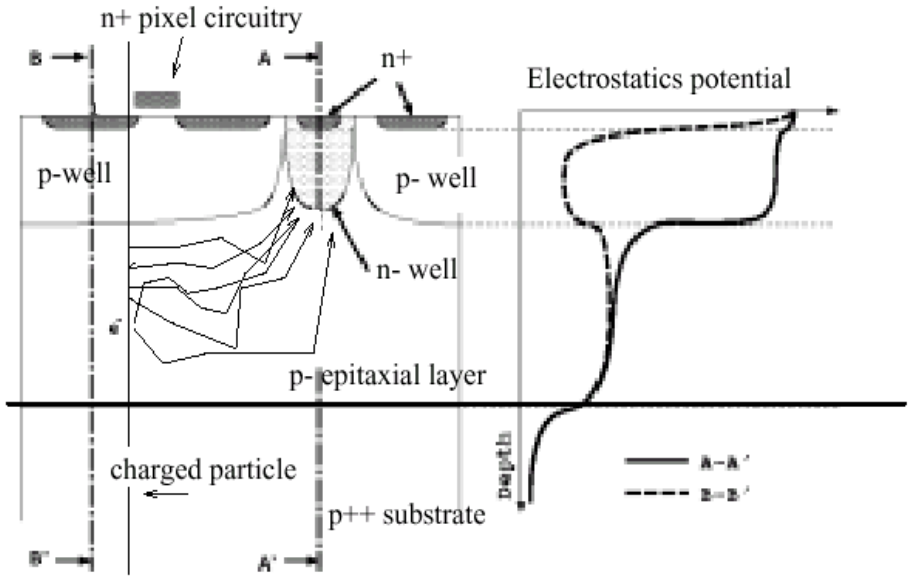
- Copy LEPSI style APS
- Using what is learned from the copy to investigate possible readout schemes for power and speed
  - » Possible directions: full fast data read vs on chip zero suppression

Next a look at the LEPSI MIMOSA APS design 

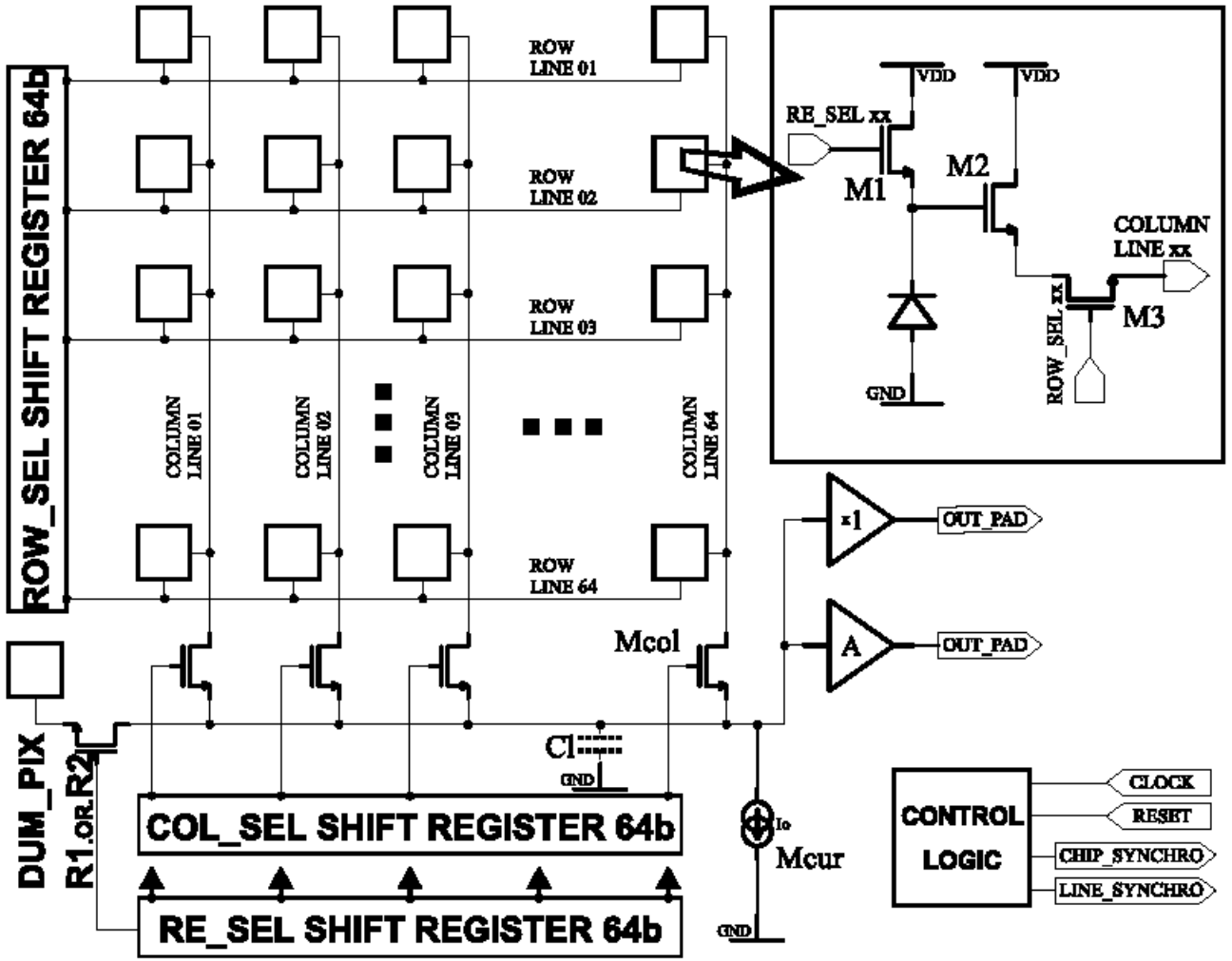
A Monolithic Active Pixel Sensor for Charged Particle Tracking and Imaging using Standard VLSI CMOS Technology

J.D. Berst, B.Casadei, G.Claus, C.Colledani, W.Dulinski, Y.Hu, D.Husson, J.P.Le Normand, R. Turchetta and J.L.Riester
LEPSI, Strasbourg
G.Deptuch, Y.Gornushkin, S.Higueret, M.Winter
IReS, Strasbourg

- LEPSI APS
  - » 20 □m square pixels
  - » 4 64X64 arrays
- MIMOSA 1, 0.6 □m CMOS
- MIMOSA 2, 0.35 □m CMOS



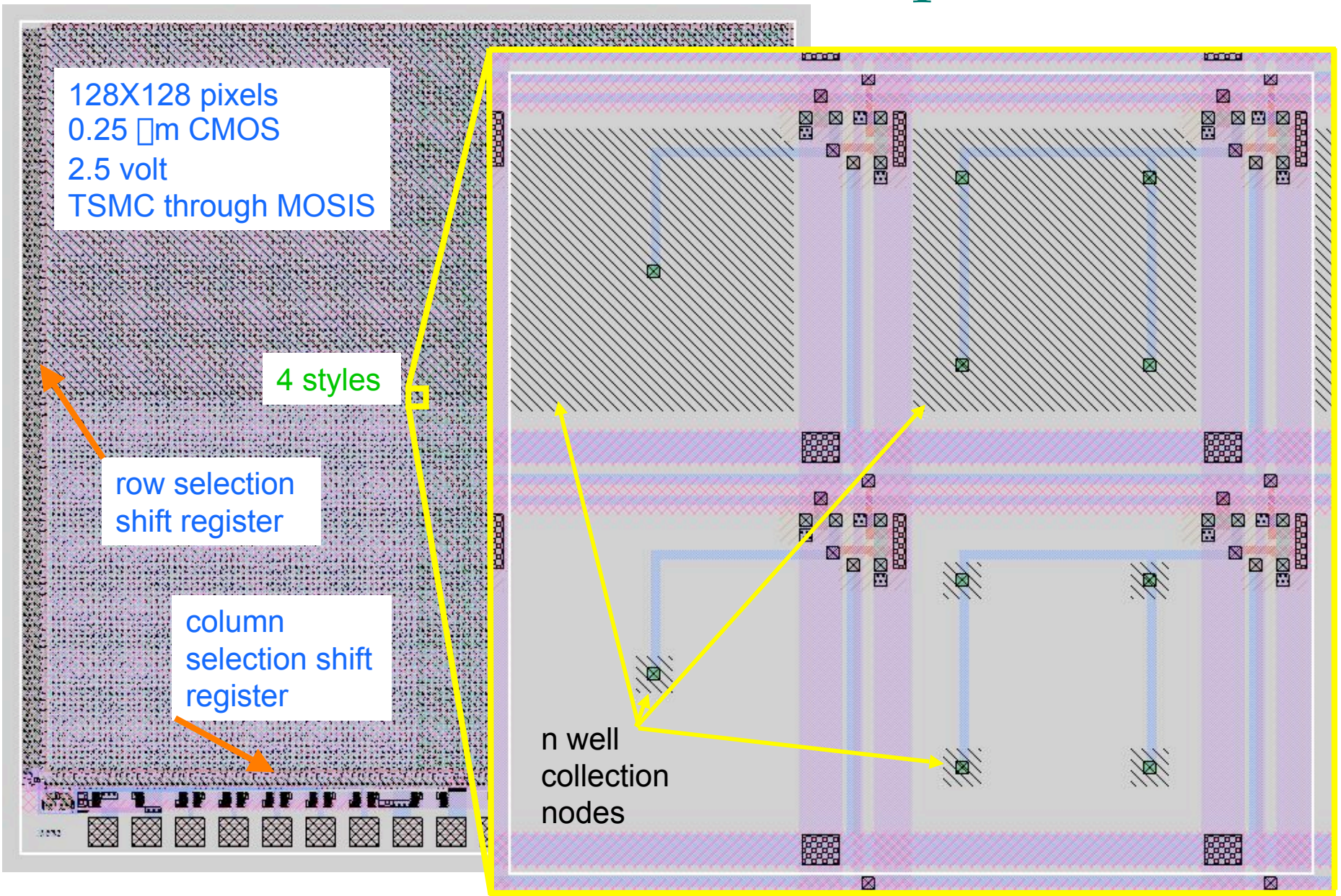
MIMOSA CHIP by LEPSI



Properties

Chip	MIMOSA I	MIMOSA II	Ours
Technology	AMS 0.6 □m	AMS 0.35 □m	TSMC 0.25 □m
Epi (□m)	14	5	8
MIP from Epi (e/h)	1100	400	440
Cn (fF)	11	7.1	6.1
Leakage I (fA)	27	0.25	0.9

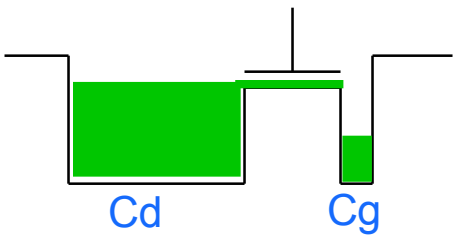
First LBNL APS chip



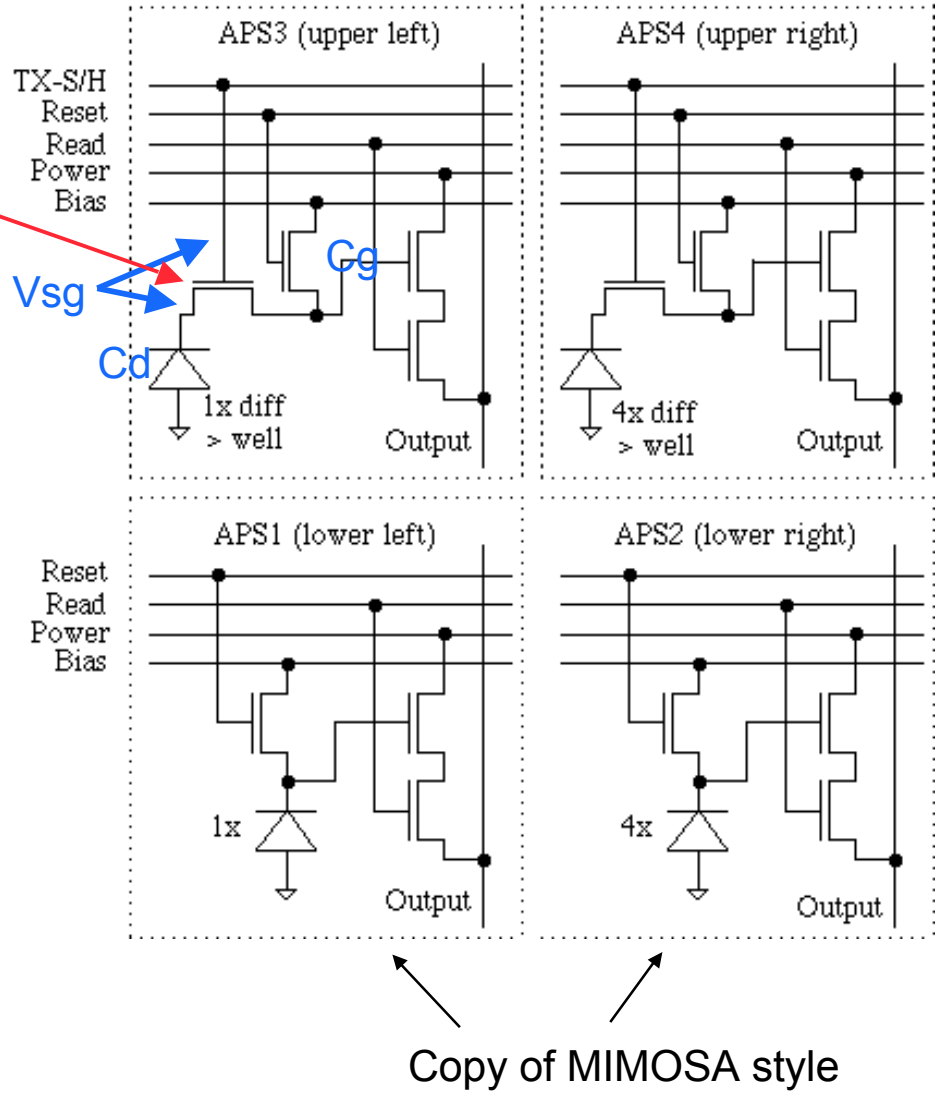
S. Kleinfelder

SK chip design

- 4 pixel styles
- Added FET acts as
  - » Sample and hold (off or on) or
  - » Capacitance isolator (TX held constant at intermediate voltage)



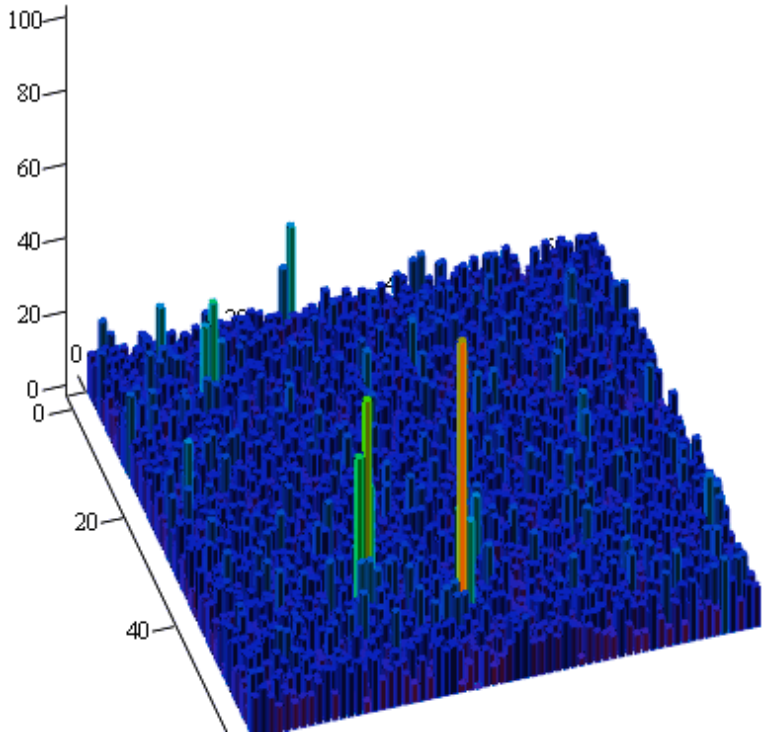
Vsg drops to Vthreshold and any additional charge spills to drain (Cg).
Only Cg is reset



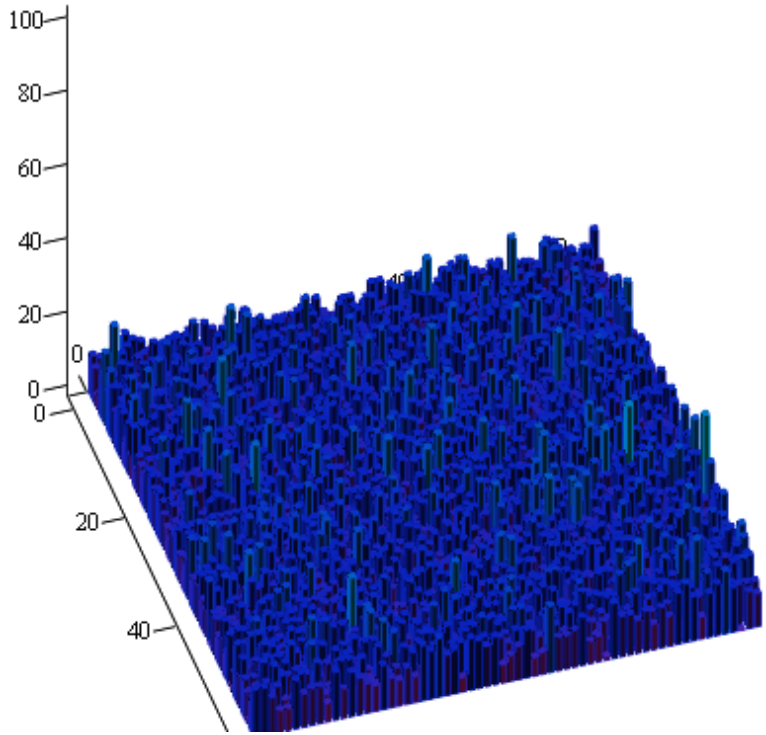
Readout like LEPSI

- Read out all pixels
- Correlated Double Sample (CDS) offline to remove Reset thermal (kTC) and Fixed Pattern noise
- Average baseline subtraction to remove leakage current pedestal

LBL APS test with 1.5 GeV/c e-beam



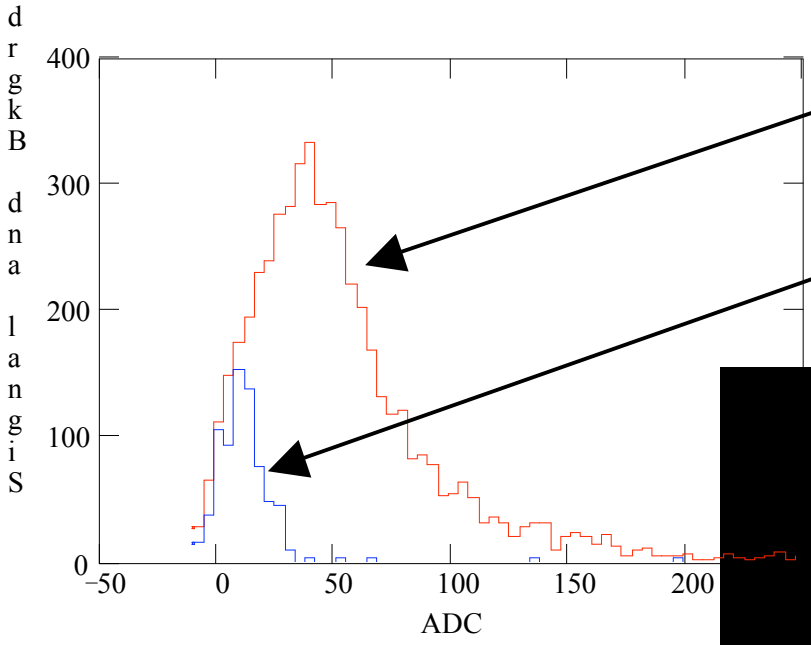
SE + 10



NE + 10

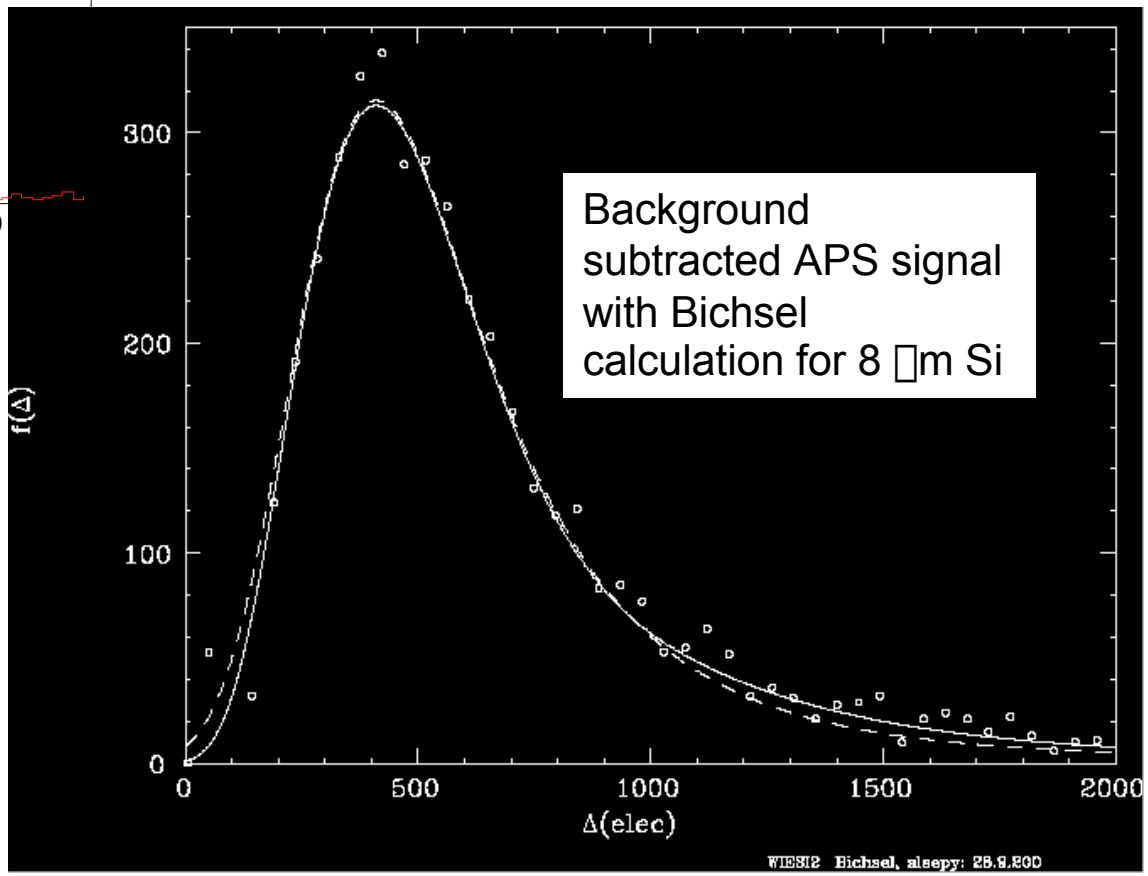
17 e RMS per pixel

LBL APS measured MIP signal



Sums of 25 pixel regions centered on pixels with ADC ≥ 7

Same sums with empty frames

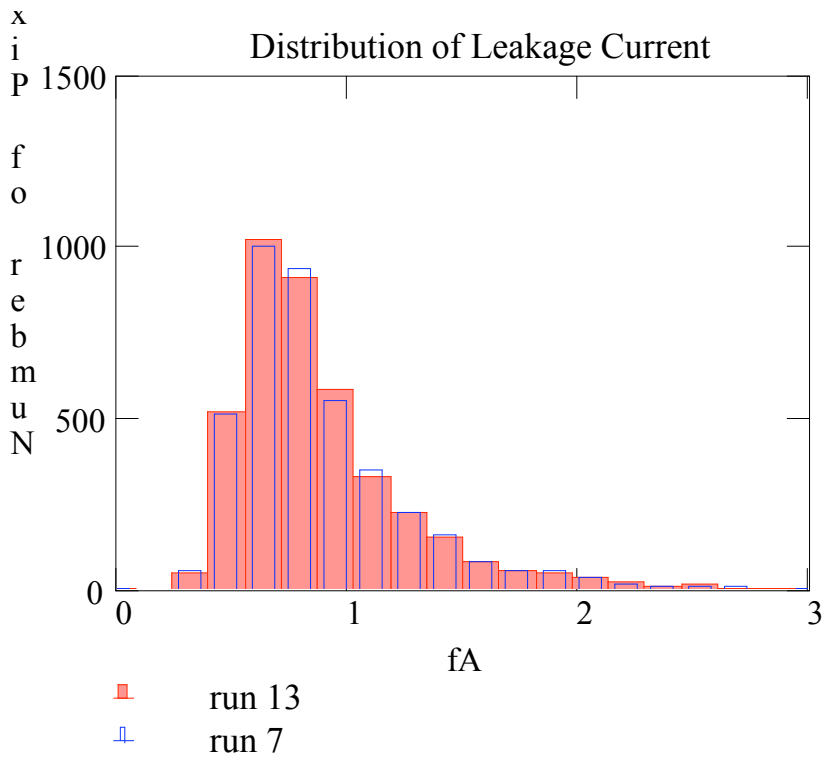


Background subtracted APS signal with Bichsel calculation for 8 □m Si

- Conclusion, signal to noise is good enough to get good efficiency without excessive false hits
- The above analysis is with CDS and leakage current subtraction

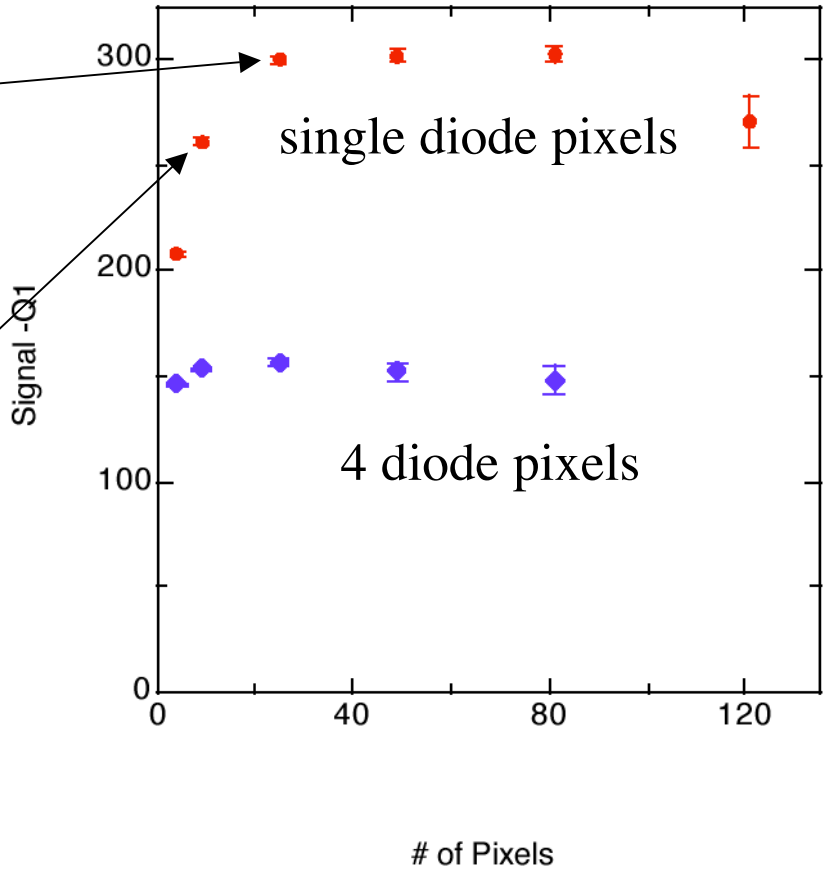
Leakage Current

- Mean pixel current 0.9 fA or 5600 e/sec
- Q leakage = 1 MIP in 70 ms
- Negligible with cooling (preliminary), i.e. won't need correction for zero suppress



Measurement of charge sharing

- 100% charge collection in center pixel + two nearest neighbors
- 85% charge collection in center pixel + nearest neighbor



Properties, LBNL APS

MIP (most probable)	440 e
Node C, measured with Fe^{55} Xray	6.1 fF
Gain	~26 □V/e
Noise (1 pixel, CDS, I_{leak} subtr)	17 e rms
Signal/Noise (9 pixel sum, CDS)	9
Signal/Noise (potential, single pix)	26
kTC reset noise (measured)	50 e rms
kTC reset noise (expected)	30 e rms
Leakage Current	0.9 fA

Development paths

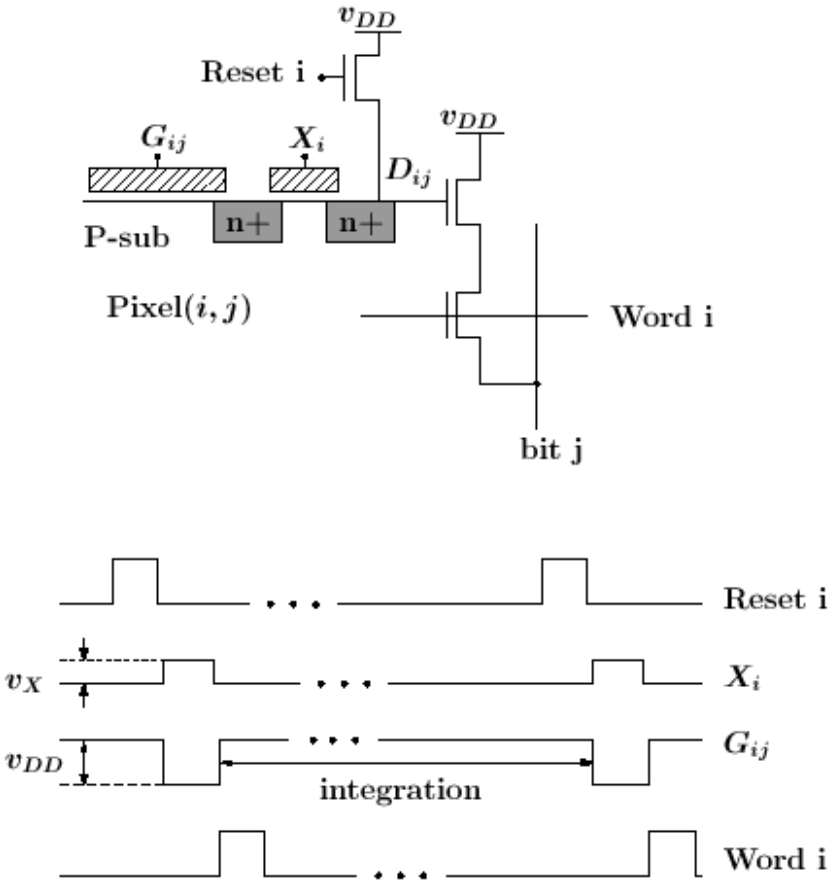
- Fast readout, no zero suppression
- Looking for zero suppression solutions
- LEPSI has built a zero suppression chip, awaiting results
- Will consider first generation using LEPSI ladder – again awaiting information on their new device

On Chip Zero suppression will require:

- Leakage current control
- Photo-gate or some trick to remove KTC noise
- Photo-gate will limit signal to one pixel

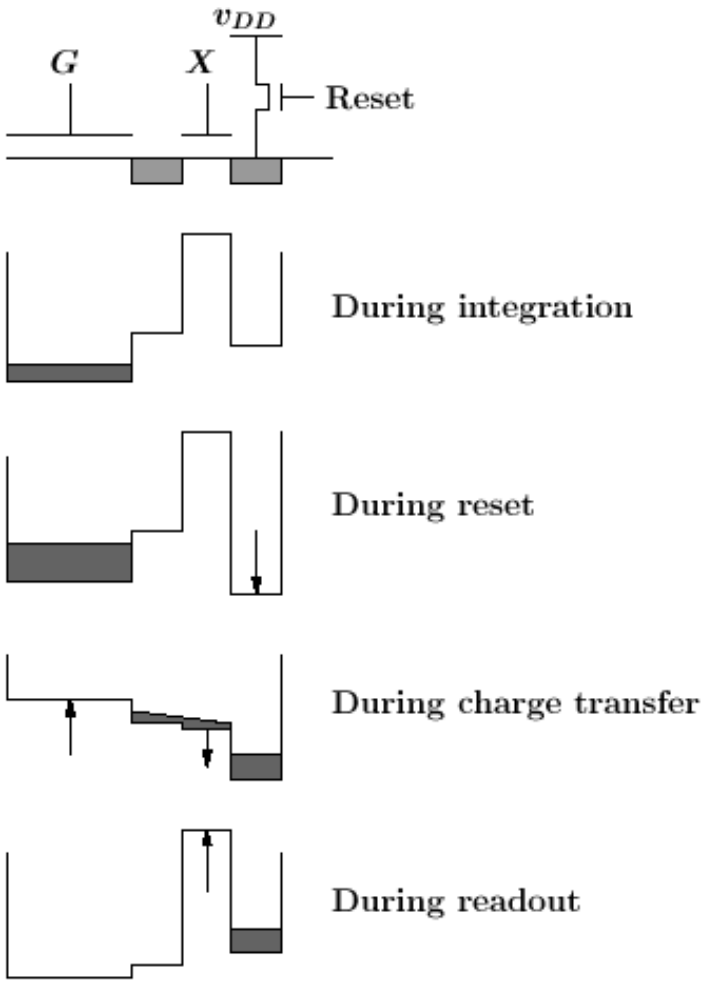
- Or will require heroic on chip CDS and current subtraction, lots of memory and processing

CMOS Photogate APS



Instructor:
Prof. Abbas El Gamal, abbas@isl.stanford.edu

Potential Well Diagram for Photogate APS



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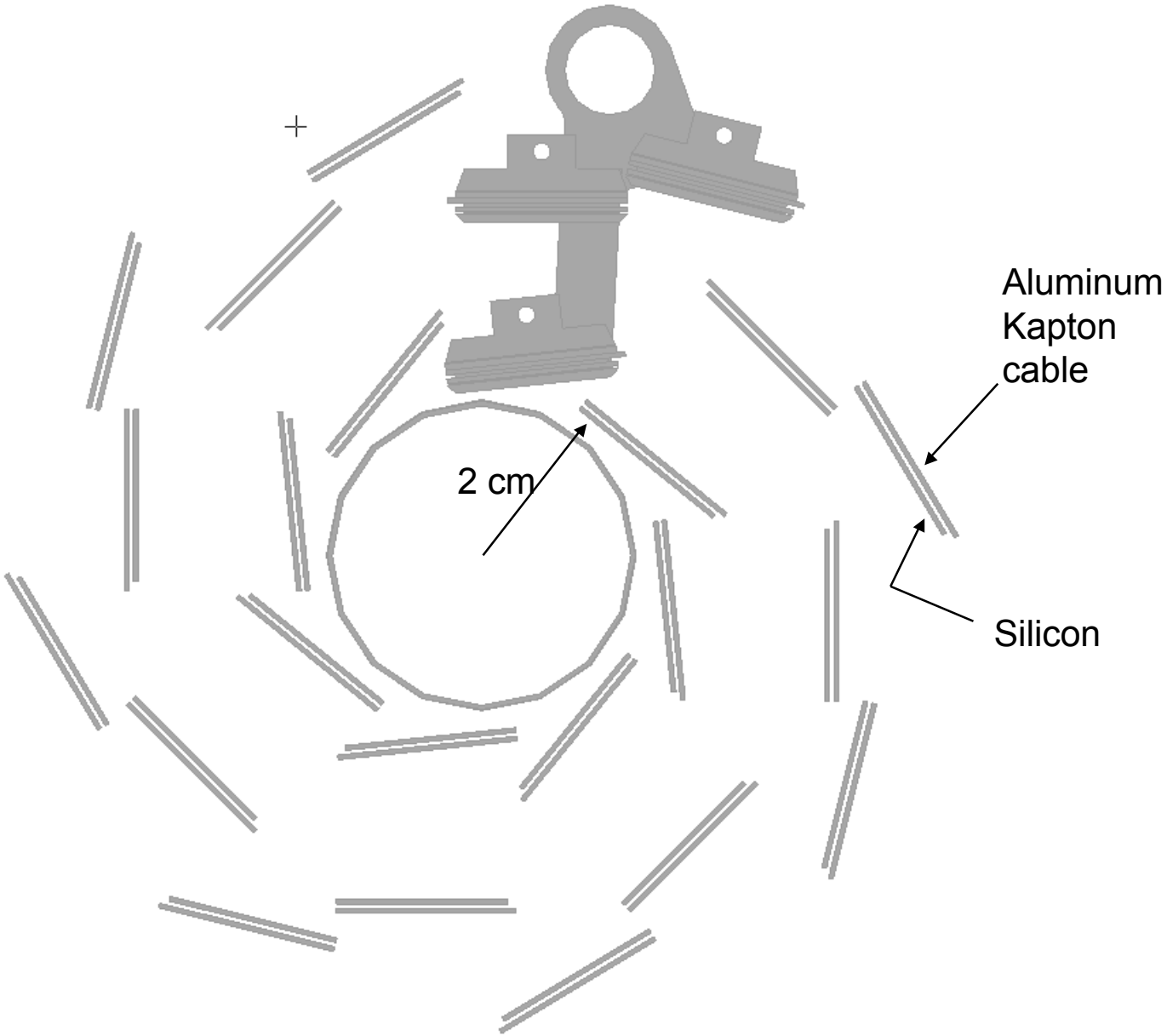
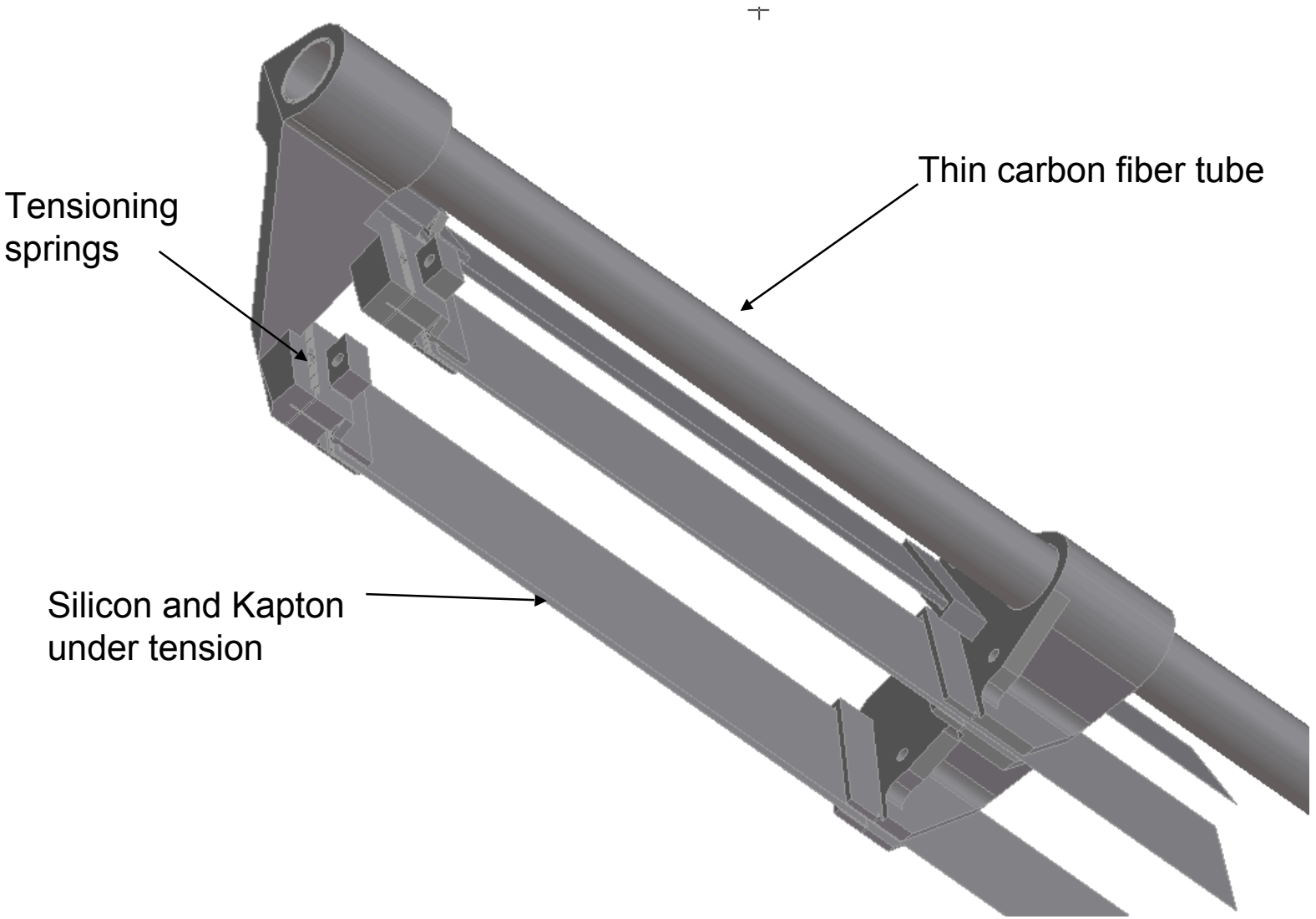
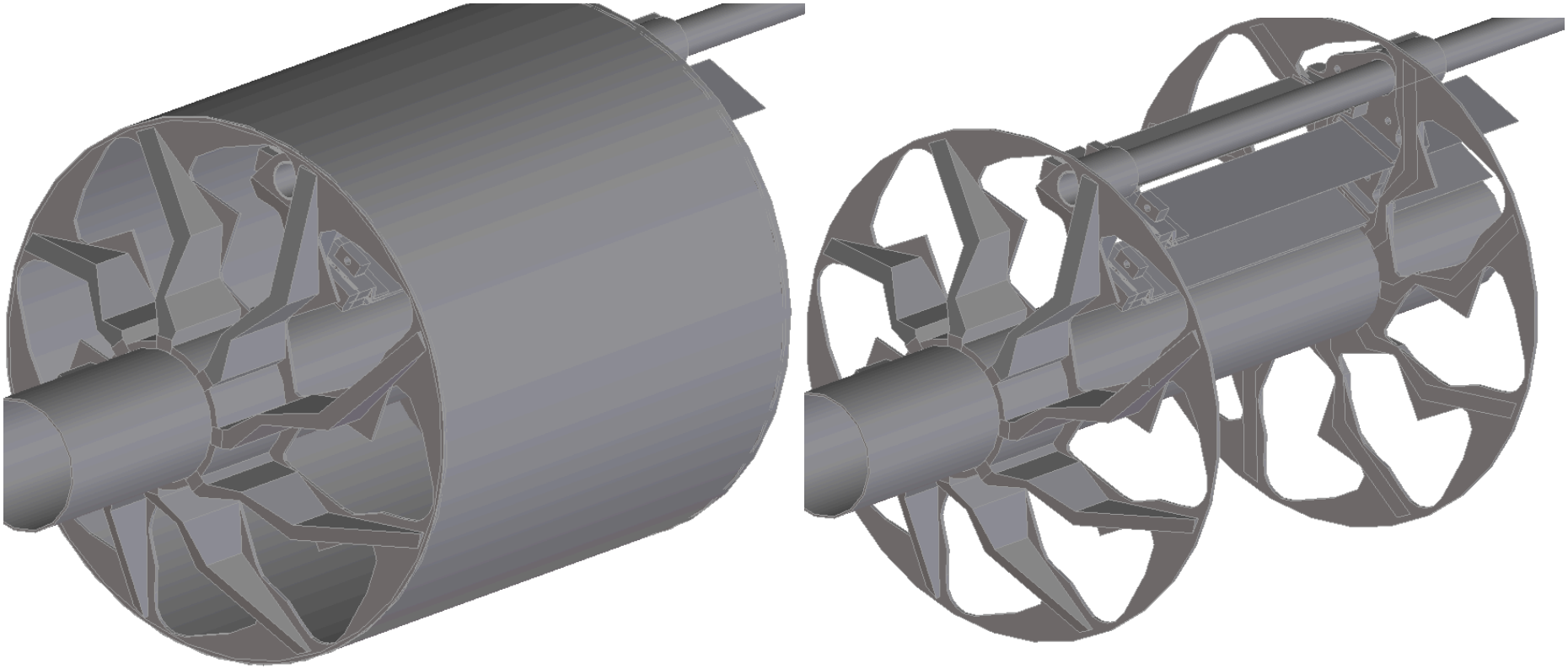
Mechanical concept



Support concept

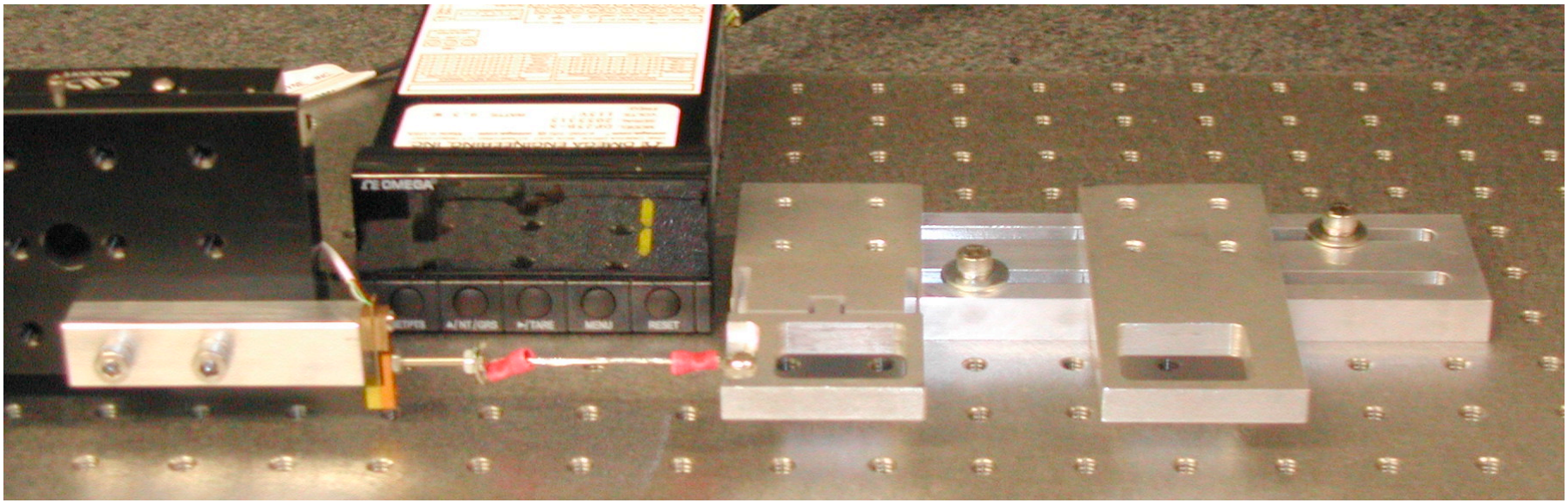


Beam pipe and support shell



Mechanical development for support and cooling of thinned silicon

- Have thinned silicon 50 □m and 100 □m cut to ladder dimensions
- Testing support and tensioning methods



Conclusion

- New challenging technology with unknowns
- Significant potential gains
- Important for STAR Long Range Plan
  - » Could benefit other RHIC experiments and heavy ion program at LHC
- ~Cost 3.25 M$
- ~Time 4-5 years

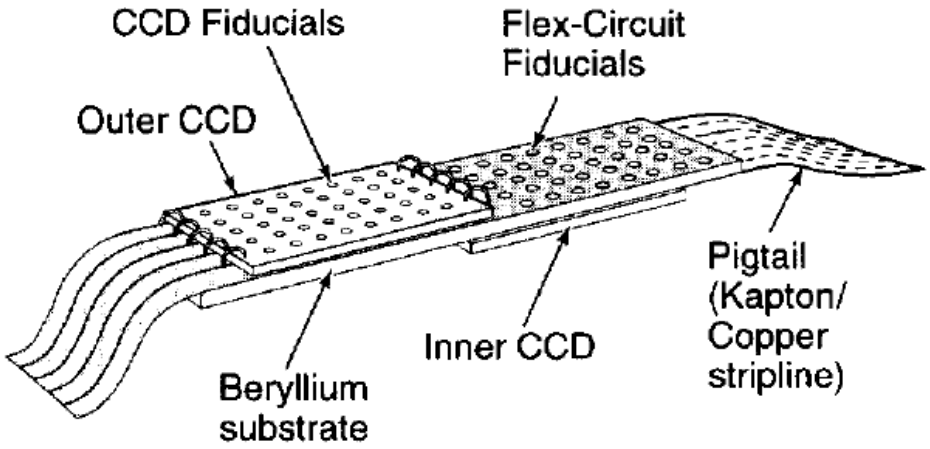
LEPSI latest progress

- Ladder? Due back soon, full size chips will be thinned to 100 □m (MIMOSA-5)
- Working on chip sparsification (MIMOSA-6)

Mechanical Possibilities beyond VXD3 ?

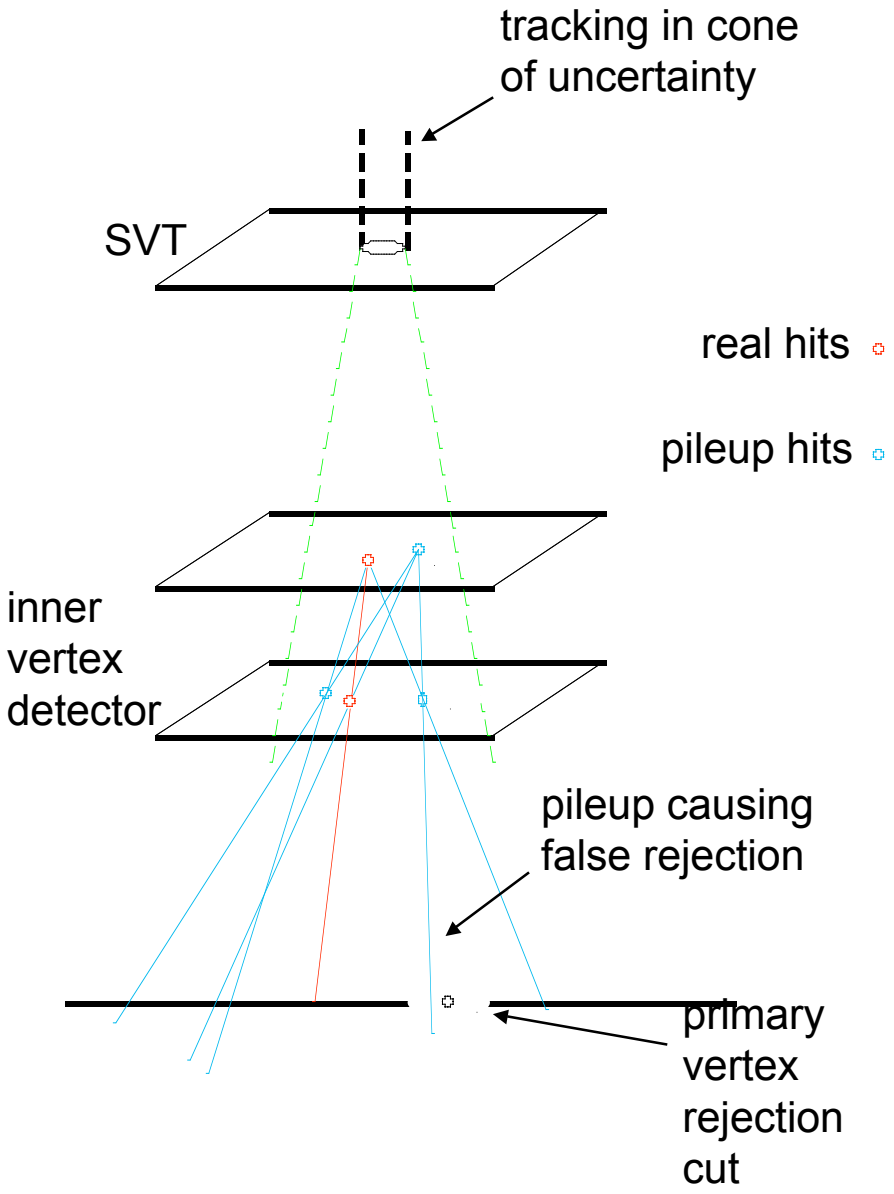
Material	VXD3		APS	
	(□m)	% X_0	(□m)	% X_0
Be Beam Pipe	760	0.22	600	0.17
Silicon	180	0.16	40	0.037
Kapton		0.05		0.05
Copper	17.8	0.09		
Aluminum			28	0.023
Be substrate	380	0.11	40	0.011
Total		0.63		0.3

VXD3 Ladder



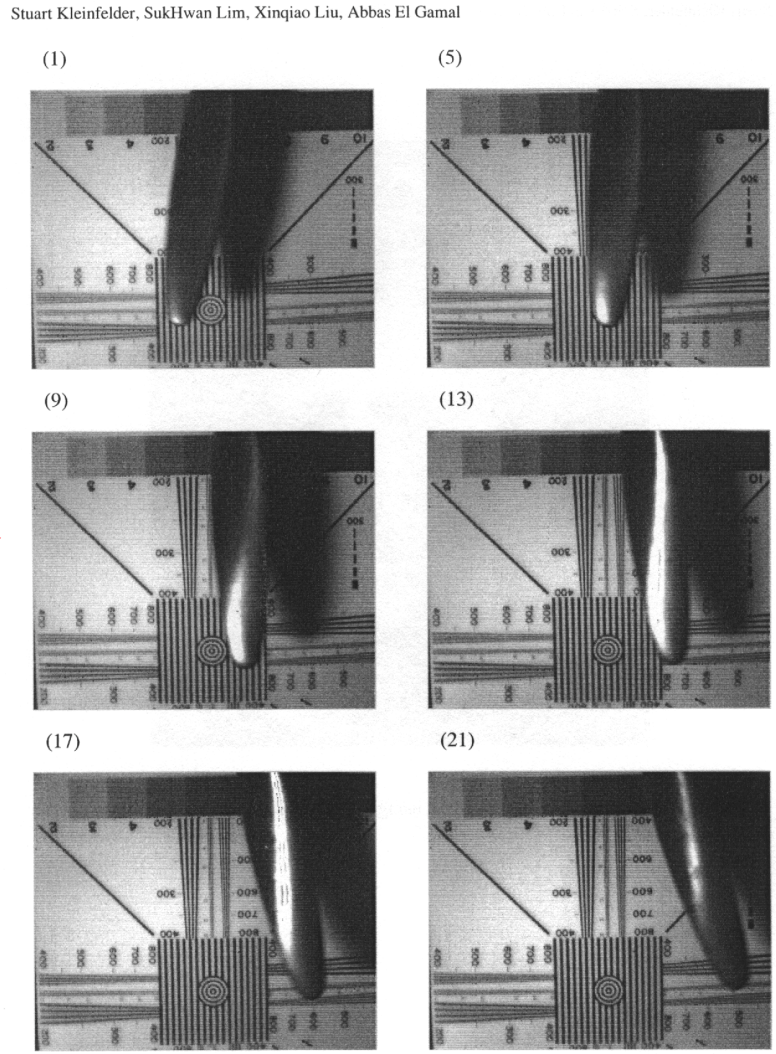
False rejection by pileup

- Purpose of vertex detector – remove primary tracks before calculating invariant mass
- 40 x design luminosity, 5 ms readout
  - » 400 hits/cm^2
  - » 1.4% pixels filled
  - » **false rejection 0.5%**
- 40 X design luminosity, 20 ms readout
  - » 1500 hits/cm^2
  - » 5.3% pixels filled
  - » **false rejection 2.9%**



APS development by Stuart Kleinfelder

- Previous experience
  - » SCA for EOS, NA49 and STAR
  - » ATWD for Amanda and KamLAND, 1 GHz FADC - for just milliwatts of power
  - » 10,000 Frame/sec video chip (thesis project)
- 1st step – reproduce LEPSI results



10,000 fps, every 4th frame displayed
propeller speed ~ 2000 rpm

Inner Vertex Detector Requirements

- Most Critical
  - » Must be thin < 0.2% X_0
  - » Must be low power < 100 mW/cm^2, gas cooling to be thin
  - » Must be minimum distance from beam, excellent two track resolution
  - » Must survive 1 year, 2 kRad
- Desirable
  - » Readout fast enough to work with RHIC X40 up grade. 5 ms to avoid too much pileup
- No interest
  - » Use in a trigger is not being considered